A Mechanism-Based Methodology for Processor Package Reliability Assessments

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ABSTRACT

Until recently, processor packages have been certified using a stress-based certification strategy. This approach, while easy to execute because the tests and end points are well defined, does not allow for an easy assessment of the fitness of the product under field applications. In fact, it doesn't require any knowledge of the end-user environment at all. The Assembly Technology Development Quality and Reliability (ATD Q&R) group has replaced this stress-based certification strategy with a mechanism-based strategy similar to one that was used extensively and successfully over many silicon technology generations. This paper describes the process by which the user environment was defined and discusses the application of this methodology to new processor package technologies.

INTRODUCTION

Intel processor packages up until now have been certified for reliability using a stress- or standards-based approach. This approach utilizes a fixed set of standard stresses of fixed durations to establish the field reliability of processor packages. It has been the standard means by which packages are certified throughout the industry. The standards are derived, or come directly from, the standards used to procure military electronics [1] and the methodology is described by Joint Electron Device Engineering Council JEDEC [2].

With the flip-chip (or C4 controlled collapse chip connect) generation of processor packages, questions concerning the use of military standards for certification were raised due to the extensive use of organic materials and the complexity of the design. It was assumed that the military standard stresses were either too severe or otherwise inappropriate for assessing these packages. These questions provided the impetus for reexamining the methodology.

There were three key motivators for reexamining Intel's processor package certification methodology. The first of these was the increasing segmentation of the processor market whereby packages are targeted for specific applications. This challenged the notion that one set of tests was adequate to address each market segment. For example, the duty cycles of server and notebook applications are significantly different and could result in overdesign or underdesign of the technology if both were required to meet the same test criteria. Moreover, because of market segmentation a processor is exposed to more environments, so an inflexible test suite may fail to adequately test specific field conditions.

The second motivator was the lifetime guarantee of military testing versus the customer's actual lifetime expectation. Given the rate of technological change, guaranteeing life to 100,000 hours seemed excessive. However, it wasn't clear what the customer lifetime expectation for a processor was since little data was available from the various market segments. In addition to an unclear lifetime expectation, it also was not clear what conditions did exist in the field that had to be met during that lifetime.

The final driver was the unclear link between the testing and the actual field use conditions, and moreover, what those conditions were. There are two conditions necessary for linking stress to life: a well defined user environment and physical models that links the environment to the accelerated stress test. In the existing stress-based methodology, neither the acceleration models nor the use conditions were clear; nor was it obvious that they were relevant to the now segmented processor market. Under these circumstances, highly accelerated tests appeared to be arbitrary, and in fact were unresponsive to new use environments.

These motivators were used to redefine ATD Q&R's certification methodology and align it to a mechanism- or knowledge-based approach. This approach is also described by JEDEC [3] but has been used at Intel only

reactively, i.e., for packaging when the stress-based requirements were not met. It generally has not been used in the industry due to its higher complexity and initial cost and the unclear definition of field lifetimes. The mechanism-based methodology requires that every failure mechanism be modeled against life with the appropriate physical model.

A related approach has been proposed by the high-density packaging user's group (HD-PUG) that attempts to define generic life models for various use conditions [4,5]. In this approach, the same acceleration models are applied but the model coefficients have been predetermined and are conservative. This approach, in essence, established more categories within a standards-based method, and because it was inherently conservative, did not achieve the full benefit of a mechanism-based approach.

This mechanism-based methodology was introduced on processor packages and is being considered by other packaging groups at Intel. The use condition methodology has already been adopted in silicon development as reliability limits have been reached in several areas. In general, the models have indicated that stress durations can be reduced, which has the direct benefit of saving package material and process costs and reducing time-to-information. It also allows greater flexibility in customizing reliability stress conditions so that they don't exceed the limits of the materials under test, which can generate test artifacts. Finally, since comprehensive models of the mechanisms are developed, they can be used to rapidly assess future extensions to the technology or to define when a technology will no longer meet the field requirements and needs to be replaced.

METHODOLOGY

In order to make the transition to a knowledge-based methodology, three things needed to be established: the lifetime expectations of the product, the environment in which the product was being used, and the tests necessary to simulate or accelerate that environment.

The lifetime expectations of the customers, both the OEM and the end user, were established by means of surveys. The surveys were conducted by market segment: server, performance PC, basic PC, and notebook; and also questioned whether the PC was for home or business use. From the survey data the expected lifetimes by market segment were established. Table 1 lists the survey areas broken into end-use conditions and OEM product qualification stress tests. The specific details of the survey are described elsewhere [6].

The surveys also asked specific questions concerning how the products are used in the field, hours of operation, on/off cycles, operating ambients, expected duty cycle, and storage conditions. In addition, data from processor junction temperature (Tj) and design temperatures were collected by segment for establishing the operating environment over the expected lifetime. These data were compiled by customers and used to develop use environments (or use conditions) by segment. The value or range chosen for each use condition captured approximately eighty percent of the total range of customer inputs for that condition and is therefore conservative, but not worst case. Extreme values, those beyond meteorologic possibility, were excluded.

Table 1: Survey questions

Use Conditions	Stress Tests
system lifetime	bake testing
cycles/Week (on/off) plus suspend/resumes	temperature cycling
on time hours per week	humidity testing
drop height	shock testing
use ambient range	drop testing
use humidity range	vibration testing
use/shipping vibration	
use/shipping shock	
storage temperature range	
storage humidity range	

Once the ambients were established from customer input, each was assigned to various accelerated test tools. Each accelerated test has an industry-accepted physical model that can link the test to the stress condition. These models were used to define the appropriate stress conditions and durations specific to the material set and failure mechanism being assessed.

Finally, in order to ensure customer acceptance of this methodology, it was necessary to develop support within the industry for the change through Sematech and to communicate the message to the customers. The Sematech Reliability Technical Advisory Board (RTAB) filled that role.

RESULTS

Lifetime Estimates

Figures 1 and 2 represent the summarized lifetime expectations for both OEMs and end users respectively. These data form the first key portion of a mechanism-

based certification methodology, namely, establishing the lifetime expectation.

Figure 1 is a summary of the expected lifetimes by market segment based upon input from the OEM survey. From the data it can be seen that, in general, there is little lifetime differentiation across the various market segments. The expected lifetime for all segments is in the seven year range, which was a surprising result. It was assumed that servers and notebooks would differ significantly in expected life, and while there was a small difference of less than one year noted, it was not deemed significant enough to warrant establishing a separate lifetime for notebooks.

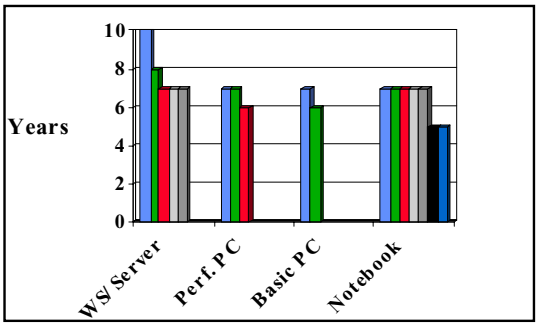

Figure 1: OEM Lifetime expectation by market segment; bars represent individual OEMs

Figure 2 is a lifetime model developed from the survey that asked end users the vintage of the processor in the computer they currently used. From that data it was possible to estimate the system replacement rate. In developing the model, an assumption was made that no replacement took place in the first three years of operation after which there was a twenty-eight percent replacement rate per year. The fitted model indicates that seventy-five percent of systems are replaced by year seven and ninety percent by year ten.

What is important to note here is that both the end user and OEMs expected lifetimes are very similar. Based on these data, the current expected lifetime for processor products was set at seven years with a small portion of the population remaining in service at ten years. Both numbers are important when modeling the wear out behavior of various failure mechanisms. Testing is taken out to a ten year equivalent to ensure that there are no catastrophic wear out mechanisms, that is, ones with narrow failure-rate distributions that result in a large proportion of the population failing over a short period of time.

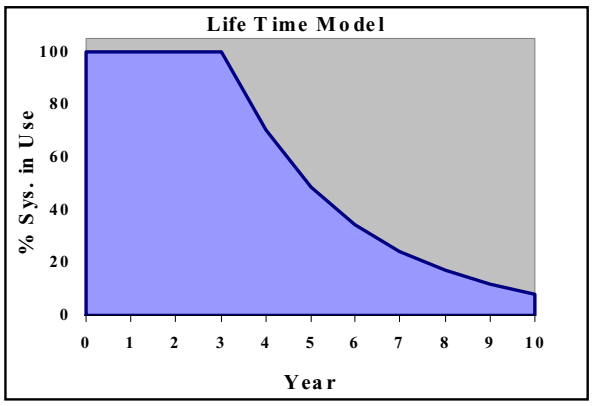

Figure 2: Lifetime model based on end-user input

Environment Definition

In Table 2, the input from the customer survey was analyzed and used to develop an environmental model. The environment takes into account the product exposure from the time it leaves Intel's manufacturing operation until the end of its useful life. Storage was broken out into two separate exposures covering two different environments. This was done since the accelerated test linkage for each category was different. The same was done for thermal and power cycles.

One of the surprising aspects of the input received was that there was little differentiation by market segment. In general, the stress on notebooks was found to be more severe than on stationary stystems for thermo-mechanical exposures such as thermal or power cycles. Notebooks were also more likely to have longer temperature-humidity-bias exposures due to short duty cycles and power save features. Servers, as expected, were at the other extreme with long duty cycles but fewer thermo-mechanical cycles. These differences were the exception however, and since processor products can be used in multiple market segments, the widest range is typically used when defining the stress conditions.

Table 2: Environmental exposures based on OEM input

Use Environment	Equivalent Use Condition by Market Segment*
moisture uptake in manufacturing	1 week out of bag
short duration extreme ambient temperature exposures during shipping and transport	-45 C to +75C for up to 24 hours
slow thermal cycles due to ambient changes or local heat sources (power supplies)	NB: 3000 cycles DT/Server/WS: 1500 cycles
fast processor On/off (to max. Tj) power cycles (including power save features)	Server/WS 3500 cycles DT/NB: 7500 cycles
operating air temperature range	10-35 C
ambient moisture during low-power state at operating voltages	62K hrs at 30C/85%RH
high operating temperature (Tj max at max. ambient)	62K Hrs
shipping vibration	Random
shipping shock or drop	0.5 m equivalent
operating vibration	Random
operating shock or drop	0.5 m equivalent
maximum sustained storage temperature	45 C Up to 1 year
minimum sustained storage temperature	-10 C Up to 1 year
socketings	15x max.
surface mount temperature exposures	3x @220C

* NB = notebook, DT = desktop, WS = workstation

Each of the environments in Table 2 were linked to the appropriate accelerated tests. The equivalent use condition from Table 2 and the lifetime model are used with acceleration models to define the accelerated test stress durations for each failure mechanism discovered during development. (The acceleration factor is the ratio of the failure rate in stress to the failure rate in the use environment.)

To ensure that future changes to the environment are comprehended and revisions made as appropriate, the survey will be repeated every two years with the OEMs. In addition, an internal review will be held for every new package technology being developed to address the detailed environment specific to that technology.

STRESS MODELS

The stress models used to link the environment and the accelerated tests were chosen because of their wide acceptance within the semiconductor packaging industry. The models in Table 3 are the baseline models being used for processor packages today and have been published in white papers by both Sematech's RTAB and Intel [7,8]. The methodology described here, however, does not preclude using other models when necessary. The Sematech models are only being used as a guide and will be modified according to the mechanism.

With the stress models' lifetime and environments defined, it becomes possible to use acceleration models to establish the expected field lifetime for every failure mechanism uncovered during development. The larger ramifications are 1) the failure models can be used to predict the impact of changes in the environment, for example, increased junction temperature effects on flip-chip (C4) joint resistance and 2) technology limits can be better defined and used for technology roadmap planning, for example, flip-chip bump pitch decreases limited by flip-chip metallurgy. With a stress-based methodology, these are not readily accomplished.

Failure Mechanism Modeling

Figure 3 gives the accelerations for several different flip-chip package thermal cycle failure mechanisms. In this example, the failure mechanisms are related through a power law relationship (Coffin-Manson) to an end-user environment of 1500 cycles with a ΔT of 40°C.

Table 3: Widely accepted acceleration models incorporated into the methodology

Mechanism	Model*
Temperature, Humidity Mechanisms	Peck's $TF = A_0 \times (a+bV) \times RH^{-N} \times \exp[E_a/kT]$ AF (ratio of TF values, Stress/use) = $[(a+bV_{Stress})/(a+bV_{Use})] \times (RH_{Stress}/RH_{use})^{-N} \times \exp[([E_a/k)(1/T_{Stress}-1/T_{use})]$
Thermal Effects	Arrhenius $TF = A_0 \times \exp[E_a/kT]$ AF (ratio of TF values, Bake/use) = $\exp[(E_a/k)(1/T_{Bake}-1/T_{use})]$
Temperature & Voltage Mechanisms	Eyring $TF = A_0 \times V^{-N} \times \exp[E_a/kT]$ AF (ratio of TF values, Stress/use) = $(V_{Stress}/V_{use})^{-N} \times \exp[(E_a/k)(1/T_{Stress}-1/T_{use})]$
Thermo-mechanical Mechanisms	Coffin-Manson Cycles to fail = $N_f = C_0 \times (\Delta T)^{-n}$ AF (ratio of N_f values, accelerated/use)= $N_{stress}/N_{use} = (\Delta T_{stress}/\Delta T_{use})^{-n}$

*TF = time to fail, AF = acceleration factor

Using the least accelerated mechanism with an exponent of 1.25 and a stress temperature ΔT of 150°C, (-25 to 125°C), it can be seen that approximately 400 cycles are required to simulate a lifetime. If a larger ΔT were chosen, fewer cycles would be required (300 for T/C B or –55 to 125°C). Typically, the most highly accelerated stress condition within the capability of the material set being stressed would be used to minimize the time to execute the test. By not being limited to the standard stress conditions, the advantage is that any stress condition can be chosen and the cycle count adjusted as required minimizing the risk of artifacts induced by overstressing.

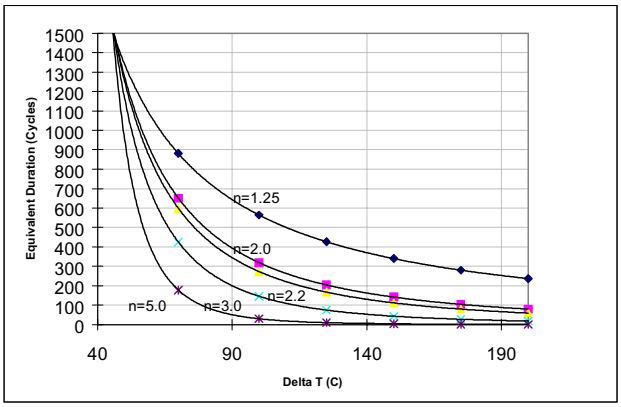

Figure 3: Thermal cycle counts at various ΔTs required to simulate 1500 environmental cycles with a ΔT of 40°C for various Coffin-Manson (power law) exponents

From this example, it can also be seen that highly accelerated mechanisms, those with exponents greater than three, only have to survive a few stress cycles. In this way, stress conditions and durations can be established for specific mechanisms while disregarding all other modes. In the stress-based-methodology, all mechanisms, regardless of acceleration, would be required to meet 1000 T/C B (ΔT = 180°C). From Figure 3, it can also be seen that requiring 1000 T/C B, as the stress-based model does, would result in designing for many lifetime multiples for highly accelerated mechanisms and would likely cost more than designed packages.

This model used a use-condition ΔT of 40°C. A key assumption was that for the flip-chip mechanisms, the only ΔT of consequence was that of the use environment. However, some thermo-mechanical failure mechanisms must be modeled from the neutral temperature of the package; that is, the temperature at which the stress in the package is zero and is typically near the molding or curing temperature. In this situation, the use ΔT will be considerably larger and will change the accelerations accordingly. Both situations should be modeled tofind the best fit, ensuring that the appropriate model is used. For a more thorough treatment of this point, see Reference 10.

In this second example, flip-chip interconnects were found to increase in resistance during bake. Flip-chip packages were baked at various temperatures and

periodic measurements of bump resistance were made. These measurements were used to establish the activation energy for this mechanism. The calculated activation energies for several different package types and vehicles ranged between 0.9 and 1.6eV with a best estimate of 1.3eV [11].

An analysis of DT system-operating temperatures was conducted and compared to actual measured system data and was found to be below 80°C [12]. The predicted mean and three sigma use-condition temperatures were used in an Arrhenius relationship with the failure-rate distribution and activation energy to estimate the time to 1% failure. From this analysis it was apparent that the lifetime at an upper operating temperature of 80°C was acceptable. Extrapolations of these results to higher operating temperatures indicated however that the lifetime needed to be increased. Thus, the acceleration models can be used for establishing a success criteria for the lifetime improvement team.

In the previous temperature cycle example multiple failure mechanisms were modeled. During temperature cycling, devices under test (DUT's) will fail for various failure mechanisms, each with a characteristic acceleration. The raw failure rates need to be transformed into use-condition fail rates using the appropriate acceleration factors. Mechanisms that fail early in stress may have long use condition lifetimes when transformed due to large acceleration factors. The transformed fail- rate models for each mechanism are summed up in a predicted cumulative lifetime fail-rate model, which is then compared against the lifetime expectation for the product and market segment.

ISSUES

There are a number of issues associated with the implementation of this methodology and to an extent these issues until now have precluded wide acceptance of this methodology. For the methodology to be successful, it requires that there be capability and capacity for running multiple stress conditions; three or more for each type of stress to be modeled. There is significant overhead for maintaining these facilities.

Several new thermal cycle conditions were defined to support the modeling of thermo-mechanical failure mechanisms adding to thermal cycle condition B and C already in use. The ranges of the new conditions overlap so that the failure mechanisms can be characterized both for Tneutral and Tstress. Table 4 lists the new conditions.

Table 4 : Thermal cycle ranges used for characterizing processor packages

Designator*	Temperature Range	ΔT
C	-65 to +150C	205C
B	-55 to +125C	180C
R	-25 to +125C	150C
Q	-25 to +100C	125C
T	0 to +125C	125C
S	0 to +100C	100C

*R, Q, T & S are internal to Intel and not published in JEDEC or Mil. Std. 883D documents.

Concomitant with multiple stress conditions is the need for the time and product volume necessary for developing acceleration models. The least accelerated legs of the testing can take months to accomplish and may require larger sample sizes due to low failure rates. The highly accelerated legs are then heavily relied upon for extrapolated estimates of the lifetime, which introduces significant uncertainty into the lifetime estimates. Since three or more conditions are run to develop a high-confidence model, three times the volume of product needs to be run to properly populate the stresses.

Highly accelerated tests run two major risks: that of introducing artifacts that wouldn't occur under less accelerated testing, and competing mechanisms. Artifacts require an increase in the failure analysis resources necessary to identify all the failure mechanisms. A comparison of failure modes between highly and less highly accelerated legs of a test sequence will identify which ones are artifacts, and these can be removed from consideration. More insidious is the risk of competing mechanisms that artificially depress a fail rate. Fab process 802 exhibited a corrosion mechanism during low- acceleration testing (85°C/85% RH) that was not seen in highly accelerated stress testing (HAST) [13]. The passivating effect of the highly accelerated test masked a failure mechanism that posed a significant field reliability risk. If the experimental design includes a sufficiently broad range of conditions, this risk should be minimized.

Customer and Industry Acceptance

Industry acceptance by semiconductor manufacturers was a key element in making this transition. Ensuring acceptance through the industry forums prevented competitors from using reliability methods as a competitive tool. One of the key forums was the

Sematech RTAB where the various manufacturers collaborated on the industry models and lifetime environmental exposures. The role of the RTAB was to reach consensus on the methodology, environment, and the method of communication to the customer base. The Sematech RTAB white paper was written and published jointly with other manufacturers and announced in a press release to industry trade journals [14,15]. Overall, acceptance by the industry has been excellent.

Intel's major customers were visited and given a presentation on the change to the methodology. The visits were timed to major product releases by market segment and served the purposes of informing the customer of the changes and of soliciting further feedback on the methods. None of the customers visited had any negative input, and most viewed the change positively. Customers whose input differed from the lifetime model presented typically asked where their specific input fell relative to other OEMs. Upon discussion of the data, none expressed significant concern that their input was different.

CONCLUSIONS

Based upon customer survey input, the expected lifetime for processor packages across all market segments was found to be seven years with a population still in service at ten years. Customer survey input was also used to define the user environment. More accurate processor package field lifetime estimates and risk assessments can be made based upon the lifetime and environmental models. This work has reestablished the link between the accelerated test methods and the field-use conditions. Through industry collaboration and customer communication, a new methodology for certification of processor packages based upon reliability failure mechanisms has been successfully implemented.

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